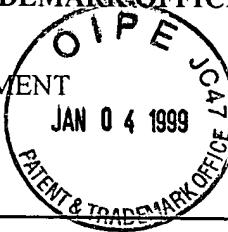


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ATTY. DOCKET NO.  
HARI.006USSSERIAL NO.  
09/129,675APPLICANT  
ELIYAHOU HARARI et al.FILED  
August 5, 1998GROUP  
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*EXAMINER INITIAL		DOCUMENT NUMBER								DATE	NAME	CLASS	SUB CLASS	FILING DATE
at	A5	4	0	9	0	2	5	8		5/16/78	Cricchi	365	184	
.	A6	4	1	4	9	2	7	0		4/10/79	Cricchi et al.	365	222	
.	A7	4	1	8	1	9	8	0		1/1/80	McCoy	365	45	
.	A8	4	2	5	3	0	5	9		2/24/81	Bell et al.	RECEIVED	714	721
.	A9	4	2	7	2	8	3	0		6/9/81	Moench	MAR U	365	45
.	A10	4	2	7	9	0	2	4		7/14/81	Schrenk	365	185.22	
.	A11	4	2	8	7	5	7	0		9/1/81	Stark	GROUP	2365	104
.	A12	4	3	9	3	4	7	5		7/12/83	Kitagawa et al.	365	185.21	
.	A13	4	4	1	5	9	9	2		11/15/83	Adlhoch	365	94	
.	A14	4	4	6	0	9	8	2		7/17/84	Gee et al.	365	185.19	
at	A15	4	4	9	5	6	0	2		1/22/85	Sheppard	365	104	

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		DOCUMENT NUMBER								DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
at	B1	GB	2	0	6	1	6	5	1	5/1981	United Kingdom	611C	7/00	
.	B2	GB	2	0	2	9	1	4	5	3/1980	United Kingdom	611C	17/00	
.	B3	JP	6	2	2	5	7	6	99	11/1987	Japan	611C	17/00	Abstract
.	B4	JP	5	9	3	1	1	5	8	2/1984	Japan	B32B	035/00	Abstract
at	B5	DE	3	6	3	7	6	8	2	5/1987	Germany	611C	17/00	Abstract

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

at	C1	Bleiker et al., "A Four-State EEPROM Using Floating-Gate Memory Cells", IEEE Journal of Solid-State Circuits, vol. sc-22, No. 3, June 1987, pp. 460-463.
at	C2	Torelli et al., "An Improved Method for Programming a Word-Erasable EEPROM", Alta Frequenza, Vol. 52, Nov. - Dec. 1983, no. 6, pp. 487-494.
at	C3	Stark, "Two Bits Per Cell ROM", Digest of Papers of Spring COMPCONS 81, Feb. 23-26, VLSI LABORATORY, pp. 209-212.

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*Anderson*

## DATE CONSIDERED

07/26/01

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ATTY. DOCKET NO.

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*EXAMINER INITIAL		DOCUMENT NUMBER								DATE	NAME	CLASS	SUB CLASS	FILING DATE
at	A16	4	5	8	6	1	6	3		4/29/86	Koike	365	104	
	A17	4	6	1	2	6	2	9		9/16/86	Harari	365	185.08	
	A18	4	7	1	8	0	4	1		1/5/88	Baglee et al.	365	185.22	
	A19	4	7	3	3	3	9	4		3/22/88	Giebel	714	711	
	A20	4	7	5	2	9	2	9		6/21/88	Kantz et al.	714	719	
	A21	4	7	6	3	3	0	5		8/9/88	Kuo	365	185.22	
	A22	4	7	7	9	2	7	2		10/18/88	Kohda et al.	714	721	
	A23	4	7	9	9	1	9	5		1/17/89	Iwahashi et al.	GROUP 2365	185.21	
	A24	4	8	0	7	1	8	8		2/21/89	Casagrande	365	185.05	
	A25	4	8	0	9	2	3	1		2/28/89	Shannon et al.	365	201	
at	A26	4	8	1	1	2	9	4		3/7/89	Kobayashi et al.	365	185.22	

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		DOCUMENT NUMBER								DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)
at	B6	DE	3	8	3	1	5	3	8	3/1989	Germany	611C	17/06	Abstract
	B7	JP	62	1	8	8	1	0	0	8/1987	Japan	611C	17/00	Abstract
	B8	JP	0	1	2	3	8	7	8	5/1989	Japan	611C	11/34	Abstract
at	B9	JP	0	1	4	6	9	4	9	10/1989	Japan	611C	11/34	Abstract

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

at	C4	Furuyama et al, "An Experimental 2-BIT/CELL Storage Dram for Macro Cell or Memory-on-Logic Application", IEEE Custom Integrated Circuits Conference, May 1988, pp. 4.4.1 - 4.4.4
at	C5	Krick, "Three-State MNOS FET Memory Array", IBM Technical Disclosure Bulletin, Vol. 18, No. 12, May 1976, pp. 4192-4193.
at	C6	Alberts et al, "Multi-Bit Storage Fet Earom Cell" IBM Technical Disclosure Bulletin," Vol. 24, No. 7A, Dec 1981, pp. 3311-3314, 4193.

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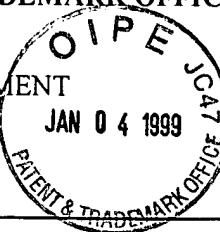
HARI.006USS

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August 5, 1998

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*EXAMINER INITIAL		DOCUMENT NUMBER								DATE	NAME	CLASS	SUB CLASS	FILING DATE
at	A27	4	8	4	7	8	0	8		7/11/89	Kobatake	365	104	
	A28	4	8	7	0	6	1	8		9/26/89	Iwashita	365	185.18	
	A29	4	9	4	3	9	6	2		7/24/90	Imamiya et al.	365	930.08	
	A30	4	9	5	6	8	1	6		9/11/90	Atsumi et al.	365	185.22	
	A31	4	9	9	9	8	1	3		3/12/91	Ohtsuka et al.	RECV'D 365	185.18	
	A32	5	0	0	3	5	1	0		3/26/91	Kamisaki	MAR 6 365	187.01	
	A33	5	0	5	3	9	9	0		10/1/91	Kreifels et al.	711	103	
	A34	5	0	9	5	3	4	4		3/10/92	Harari	GROUP 22700	328	
	A35	5	1	6	3	0	2	1		11/10/92	Mehrotra et al.	365	185.03	
	A36	5	2	9	7	1	4	8		3/22/94	Harari et al.	714	710	
at	A37	5	3	5	7	4	6	2		10/18/94	Tanaka et al.	365	185.22	

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		DOCUMENT NUMBER								DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

at	C7	Horiguchi et al., "An Experimental Large-Capacity Semiconductor File Memory Using 16-LEVELS/CELL Storage" IEEE Journal of Solid-State Circuits, Vol. 23, Feb 1988, No. 1, pp. 27-33.
at	C8	Masuoka et al., "A 256-KBIT Flash EEPROM using Triple-Polysilicon Technology" IEEE Journal of Solid-State Circuits, vol. SC-22, no. 4, pp 548-552, New York, US, August 1987
at	C9	Berenga et al., "E2-PROM TV Synthesizer", 1978 IEEE International Solid-State Circuits Conference: ISCC 78, February 17, 1978, pp.196-197.

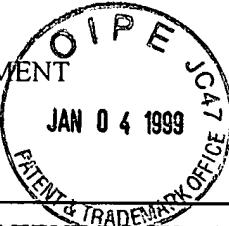
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FORM PT01449 (REV. 8-83)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE								ATTY. DOCKET NO. HARI.006USS	SERIAL NO. 09/129,675
INFORMATION DISCLOSURE STATEMENT										APPLICANT ELIYAHOU HARARI et al.	
<i>(Use several sheets if necessary)</i>										FILED August 5, 1998	GROUP 2785 2824



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*EXAMINER INITIAL		DOCUMENT NUMBER							DATE	NAME	CLASS	SUB CLASS	FILING DATE
at	A38	5	3	6	1	2	2	7	1/1/94	Tanaka et al.	365	185.22	
	A39	5	6	0	2	9	8	7	2/11/97	Harari et al.	714	8	
	A40	4	9	5	9	8	1	2	9/25/90	Momodomi et al.	365	185.17	
	A41	4	9	3	9	6	9	0	7/3/90	Momodomi et al.	365	185.17	
at	A42	4	9	9	6	6	6	9	2/26/91	Endoh et al.	365	185.17	
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## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER							DATE	COUNTRY	CLASS	SUB CLASS	TRANS.? (YES/NO)

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent pages, Etc.)

at	C10	Kynnett et al., "An In-System Reprogrammable 32K X 8 CMOS Flash Memory", IEEE Journal of Solid-State Circuits, Vol. 23, No. 5, Log Number 8822443, October 1988, pp. 1157-1163.
at	C11	Klingman, "Microprocessor Systems Design" Prentice-Hall Inc., pp. 30-31, 1977.
at	C12	SGS-Ates, "Excerpts From a 1983 Data Book" SGS-Ates Group, 45 pp., Nov. 1983.
at	C13	Torelli et al, "Non-Volatile Station Memory and Remote Control Receiver and Memory-Display Driver" IEEE Transactions on Consumer Electronics, vol. CE-29, no. 3, pp. 103-113, August 1983.

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<i>Andrew</i>	07/26/01

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INFORMATION DISCLOSURE STATEMENT <i>(Use several sheets if necessary)</i>		APPLICANT ELIYAHOU HARARI et al.	
		FILED August 5, 1998	GROUP 2785 2824

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GROUP 2100

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<i>at</i>	C14	Torelli et al., "Integrating Non-Volatile Station Memory and Remote Control Receiver in a Single Chip" IEEE Digest of Technical Papers, Cat. No. 83CH1872-1, 2 pp., June 8, 1983.
<i>at</i>	C15	Caironi et al., "A TV Frequency Synthesis System With A Single Chip Microprocessor Interface Including Non Volatile Memory" IEEE Transactions on Consumer Electronics, vol. CE-28, no. 3,pp. 363-71, August 1982
<i>at</i>	C16	Torelli, "An LSI Technology Fully Compatible EAROM Cell": SGS-ATES Componenti Elettronici SpA, no. 6, vol. LI, 7 pp., 1982.
<i>at</i>	C17	Torelli et al., "PLL2K-PLL Frequency Synthesizer for 30 Programs" SGS-ATES, Technical Note #152, pp. 1-16, 1982.

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INFORMATION DISCLOSURE STATEMENT <i>(Use several sheets if necessary)</i>		APPLICANT ELIYAHOU HARARI et al.	
		FILED August 5, 1998	GROUP 2785 2824
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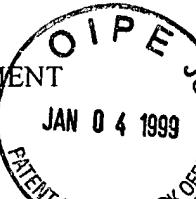
<i>at</i>	C18	Torelli et al., "Single Chip, 16-Station TV Digital Tuning System" SGS Technical Note #170, pp. 1-19, 1984.
<i>at</i>	C19	Scrocchi et al., "EPM32-Electronic Program Memory System for TV (32 Stations)"SGS-ATES, Technical Note #153, pp. 1-19, 1982.
<i>at</i>	C20	SGS-ATES, "Single Chip Non-Volatile Station Memory, PCM Remote Control Receiver and Display Driver" SGS-ATES, MOS INTEGRATED CIRCUITS/M490-M491, 24 pp. May 1983.
<i>at</i>	C21	SGS-ATES, "PLL TV Microcomputer Interface" SGS-ATES, MOS Integrated Circuits/M206, 15 pp., June 1982.

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INFORMATION DISCLOSURE STATEMENT <i>(Use several sheets if necessary)</i>				APPLICANT ELIYAHOU HARARI et al.	
		FILED August 5, 1998	GROUP 2785-2824		
U. S. PATENT DOCUMENTS					
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## **FOREIGN PATENT DOCUMENTS**

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**OTHER DOCUMENTS** (*Including Author, Title, Date, Pertinent pages, Etc.*)

<i>at</i>	C22	Gee et al., "An Enhanced 16K E2PROM" IEEE Journal of Solid-State Circuits, Vol. SC-17, No. 5, October 1982, pp. 828-832.
<i>at</i>	C23	Kynett et al., "A 90-ns One Million Erase/Program Cycle 1-Mbit Flash Memory", IEEE Journal of Solid-State Circuits, vol. 24, No. 5, October 1989, pp. 1259-1264
<i>at</i>	C24	Tanaka et al., "A 4-Mbit NAND-EEPROM with tight Programmed Vt Distribution", 1990 Symposium on VLSI Circuits, Digest of Technical Papers, pp. 105-106.
<i>at</i>	C25	IBM Technical Disclosure Bulletin, "EPROMgramming Device", Vol.29, No.9, February 1987, pp. 4145-4146.

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INFORMATION DISCLOSURE STATEMENT		APPLICANT Eliyahou Harari et al.	
# 8 /IDS	(Use several sheets if necessary)	FILED August 5, 1998	GROUP 2818 AU 2824

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INFORMATION DISCLOSURE STATEMENT		APPLICANT Eliyahou Harari et al.	
#10/IDS	(Use several sheets if necessary)	FILED August 5, 1998	GROUP 2818-AU 2824

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<i>at</i>	C26	"Bipolar/Mos Memories Data Book," <u>Advanced Micro Devices</u> , ISSN 0888-4714, pp. 6-1-6-14, 1986
<i>at</i>	C27	SEEQ Data Book 1988/89, <u>SEEQ Technology, Inc.</u> , pp. 3-1-3-7

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